REMARKS

Preliminarily, Applicants thank the Examiner for the allowance of claims 26 and 27, and the indication of allowable subject matter in claims 3 and 4.

Turning to the prior art rejections, the Examiner rejects claims 1, 2, and 5-16 as being obvious over *Brigham et al.* (US 2001/0036693) in view of Applicants' admitted prior art, as shown in Fig. 2 of the instant specification, under 35 U.S.C. § 103. Applicants respectfully traverse this rejection for the reasons set forth below.

On page 2 of the Office action, the Examiner states the following:

> Applicants have amended independent claim 1 to recite that the source and drain regions are formed above an insulator layer.
>
> As stated in the previous action, Brigham does acknowledge that, while his chosen configuration may not utilize a SOI construction, nevertheless, it is recognized in the art that ***SOI approaches do provide certain advantages*** by reducing junction capacitance that may degrade the performance of the FET. This view is further ***reinforced by applicants' own description of the prior art shown in Fig. 2***, where the formation of FINFET devices specifically, is well known in the art.
>
> Consequently, one skilled in the art would be motivated to combine these teachings so as to derive the known benefits of reduced junction capacitance in a FINFET structure formed as shown in Fig. 2. The other features of the dependent claims are also taught or within the scope of the cited references.

(Emphasis added.)

Paragraph 0023 of *Brigham et al.* discusses the various previous attempts of reducing parasitic junction capacitance, stating:

> The speed and power performance characteristics of MOSFET integrated circuits can be improved by reducing parasitic junction capacitance. Various attempts to reduce this junction capacitance have included fabricating transistors on insulating substrates, for example sapphire, or more commonly, a ***silicon-on-insulator (SOI) substrate***. While these approaches do reduce the junction capacitance associated with FET structures by isolating the junctions from the semiconductor body, ***unfortunately they also create device performance problems due to the floating body effect***.

(Emphasis added.)

Not only does *Brigham et al.* use and teach a different approach that does ***not*** use an insulator layer on the substrate, in order to avoid the floating body effect, but also explicitly ***teaches away*** from using a SOI substrate.

As stated in paragraph 0007 of the instant application, the prior art illustrated in Fig. 2 of the instant application suffers from the following deficiency:

> ... the channel region that is not protected by oxide spacers is provided with doping atoms. In the case of this underdiffusion, doping atoms pass laterally into the channel region after their implantation. Particularly in the case of short channel lengths--such as occur in the case of the known fin field-effect transistor--such underdiffusion has substantial negative effects on the control response of the field-effect transistor.

The present invention of the instant application overcomes the above noted deficiency by incapsulating the gate.

The oxide layer 202 of the prior art is mentioned only in paragraph 0003 ("FIG. 2 shows such a fin field-effect transistor 200 having a silicon substrate 201 and an oxide layer 202 made of silicon oxide SiO_2 on the silicon substrate 201.") and in paragraph 0004 ("A fin 203 made of silicon is provided on a part of the oxide layer 202."). There is no disclosure or suggestion in the description that that the oxide layer 202 offers any particular advantage. Consequently, there is ***no*** suggestion or motivation in the description of the prior art device for using a SOI substrate, and therefore for combining the prior art device of Fig. 2 with *Brigham et al.*

Considering that there is no suggestion or motivation in neither the description of the prior art device in the instant application nor in *Brigham et al.* (to the contrary!) for combining the prior art device with *Brigham et al.*, the requirements for establishing a *prima facie* case of obviousness by modifying or combining reference teachings, as required by MPEP § 2143, are not satisfied.

The invention as recited in claim 1 of the instant application is therefore patentable over the applied prior art, and because claims 2-16 are ultimately dependent on claim 1, they are patentable as well.

Reconsideration and allowance of all claims are therefore respectfully solicited.

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Respectfully submitted,

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